AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A method of driving a liquid crystal display device having a plurality of bus lines for transmitting image data, said method comprising:

branching original image data having an original data rate into branched plural-systems image data comprising plural systems having a converted data rate [[which]] that is equal to either said original data rate or a half of said original data rate;

supplying a source driver circuit with said branched plural-systems image data in ~~synchronizing~~ synchronization with at least [[a]] one clock signal having a clock frequency [[which]] that is ~~a quarter~~ less than half of said original data rate; and

allowing said source driver circuit to further branch said branched plural-systems image data into gray-scale voltage signals.

2. (currently amended) The method as claimed in claim 1, wherein [[the]] a number of said systems of said branched plural-systems image data is 2J, and

wherein J is a positive integer number.

3. (currently amended) The method as claimed in claim 1, wherein [[the]] a number of said systems of said branched plural-systems image data is 4J, and

wherein J is a positive integer number.

4. (original) The method as claimed in claim 1, wherein said converted data rate is equal to said original data rate.

5. (original) The method as claimed in claim 1, wherein said converted data rate is equal to a half of said original data rate.

6. (currently amended) The method as claimed in claim 1, wherein said at least [[a]] one clock signal comprises two clock signals different in phase by a half cycle from each other, and

wherein rising edges of said two clock signals serve as triggers to input said branched plural-systems image data into said source driver circuit.

7. (currently amended) The method as claimed in claim 1, wherein said at least [[a]] one clock signal comprises two clock signals different in phase by a half cycle from each other, and

wherein falling edges of said two clock signals serve as triggers to input said branched plural-systems image data into said source driver circuit.

8. (currently amended) The method as claimed in claim 1, wherein said at least [[a]] one clock signal comprises a single clock signal, and

wherein both rising edges and falling edges of said single clock signal serve as triggers to input said branched plural-systems image data into said source driver circuit.

9. (currently amended) A circuitry for driving a liquid crystal display device, said circuitry comprising:

a timing controller for generating image data and at least [[a]] one clock signal;

a plurality of data bus lines for transmitting said image data and at least [[a]] one clock signal; and

a plurality of source driver circuits for incorporating said image data in ~~synchronizing~~ synchronization with said at least [[a]] one clock signal and converting said image data into gray-scale voltage signals[[,]];

wherein said timing controller ~~includes~~ comprises:

a branching unit for branching original image data having an original data rate into branched plural-systems image data comprising plural systems having a converted data rate [[which]] that is equal to either said original data rate or a half of said original data rate.

10. (currently amended) The circuitry as claimed in claim 9, wherein [[the]] a number of said systems of said branched plural-systems image data is 2J, and

wherein J is a positive integer number.

11. (currently amended) The circuitry as claimed in claim 9, wherein [[the]] a number of said systems of said branched plural-systems image data is 4J, and

wherein J is a positive integer number.

12. (original) The circuitry as claimed in claim 9, wherein said converted data rate is equal to said original data rate.

13. (original) The circuitry as claimed in claim 9, wherein said converted data rate is equal to a half of said original data rate.

14. (currently amended) The circuitry as claimed in claim 9, wherein said at least [[a]] one clock signal comprises two clock signals different in phase by a half cycle from each other, and

wherein rising edges of said two clock signals serve as triggers to input said image data into said source driver circuits.

15. (currently amended) The circuitry as claimed in claim 9, wherein said at least [[a]] one clock signal comprises two clock signals different in phase by a half cycle from each other, and

wherein falling edges of said two clock signals serve as triggers to input said image data into said source driver circuits.

16. (currently amended) The circuitry as claimed in claim 9, wherein said at least [[a]] one clock signal comprises a single clock signal, and

wherein both rising edges and falling edges of said single clock signal serve as triggers to input said image data into said source driver circuits.

17. (currently amended) The circuitry as claimed in claim 9, wherein said timing controller further ~~includes~~ comprises:

a data polarity inversion determination unit for verifying whether or not a majority of bits of said branched plural-systems image data is changed in polarity; and

a data polarity inversion unit for inverting all bits of said branched plural-systems image data in polarity if it is verified that said majority of bits of said branched plural-systems image data is changed in polarity.

18. (currently amended) The circuitry as claimed in claim 17, wherein plural pairs of said data polarity inversion determination unit and said data polarity inversion unit are provided, and

wherein [[the]] a number of said pairs is ~~identical with~~ the same as a number of said systems of said branched plural-systems image data.

19. (currently amended) The circuitry as claimed in claim 17, wherein said data polarity inversion determination ~~circuit further includes~~ unit comprises:

a polarity change detecting circuit for detecting polarity change in bit units of said polarity-inverted image data from said branched plural-systems image data; and

a majority determination circuit for determining whether or not said majority of bits of said polarity-inverted image data is different in polarity from said branched plural-systems image data.

20. (currently amended) The circuitry as claimed in claim 9, wherein said timing controller further ~~includes~~ comprises:

a first latch circuit for latching said branched plural-systems image data in ~~synchronizing~~ synchronization with said at least [[a]] one clock signal and for outputting said branched plural-systems image data as first output data;

a first data polarity inversion determination circuit for inverting all bits of said branched plural-systems image data in polarity if a first polarity inversion signal has a predetermined level ~~which indicates~~ indicating polarity inversion, and ~~said first data polarity inversion determination circuit also~~ for outputting polarity-inverted image data;

a second data polarity inversion determination circuit for comparing said polarity-inverted image data and said branched plural-systems image data to verify whether or not a majority of bits of said polarity-inverted image data is different in polarity from said branched plural-systems image data, and ~~said second data polarity inversion determination circuit also~~ for outputting a second polarity inversion signal [[which]] that has a predetermined level ~~which indicates~~ indicating polarity inversion[[,]] if said majority of bits of said polarity-inverted image data is different in polarity from said branched plural-systems image data; and

a second latch circuit for latching said second polarity inversion signal in ~~synchronizing~~ synchronization with said at least [[a]] one clock signal and for supplying said first polarity inversion signal to said first data polarity inversion determination circuit.

21. (currently amended) The circuitry as claimed in claim 20, wherein said timing controller further ~~more includes~~ comprises:

a third latch circuit for latching said polarity-inverted image data in ~~synchronizing~~ synchronization with said at least [[a]] one clock signal and for supplying said polarity-inverted image data to said source driver circuits; and

a fourth latch circuit for latching said first polarity inversion signal in ~~synchronizing~~ synchronization with said at least [[a]] one clock signal and for supplying said first polarity inversion signal to said source driver circuits.

22. (currently amended) The circuitry as claimed in claim 21, wherein plural sets of said first and second data polarity inversion determination circuits and said first to fourth latch circuits are provided, and

wherein [[the]] a number of said [[pairs]] sets is ~~identical with~~ the same as a number of said systems of said branched plural-systems image data.

23. (currently amended) The circuitry as claimed in claim [[21]] 20, wherein said second data polarity inversion determination circuit ~~further includes~~ comprises:

a polarity change detecting circuit for detecting polarity change in bit units of said polarity-inverted image data from said branched plural-systems image data; and

a majority determination circuit for determining whether or not said majority of bits of said polarity-inverted image data is different in polarity from said branched plural-systems image data.

24-38. (canceled)

39. (new) The method as claimed in claim 1, wherein the at least one clock signal has a clock frequency that is a quarter of said original data rate.